Patent Application
Docket #45475-00027
99-44651

SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a semiconductor package and, more particularly, but not by way of limitation, to a semiconductor package that has a reduced thickness.

HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York, which is herein incorporated by reference.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of

electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, which has resulted in increased consumer demand. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendency, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a size of about 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

One obstacle to reducing the thickness of conventional semiconductor packages is the internal leads are as thick as the chip paddle. Under the condition that the thickness of the internal leads is identical to that of the chip paddle, the bond pads on the semiconductor chip that is mounted onto the chip paddle are positioned at a far higher level than are the internal leads, so that the loop height of the conductive wires for connecting the semiconductor chip and the internal leads is elevated. The loop height results in an increase in a wire sweeping phenomenon that is caused by pressure of an encapsulation material during encapsulation of the package components.

Previously, techniques for reducing the thickness of semiconductor packages have been utilized, such as back-grinding techniques in which a semiconductor chip is ground down before being mounted on a chip paddle. The back-grinding process, however, deleteriously affects the semiconductor chip. For example, a semiconductor chip that is thinned in this manner is apt to undergo warpage, which may result in damaging the internal integrated circuits. In addition, the semiconductor chip itself may be cracked during the back-grinding.

SUMMARY OF THE INVENTION

The present invention provides a semiconductor package that is extremely thin without the need for conducting a back-grinding process or at least for reducing the amount of back-grinding that is required. In one embodiment of the present invention, there is provided a semiconductor package comprising a semiconductor chip provided with a plurality of bond pads, a chip paddle bonded to the bottom surface of the semiconductor chip via an adhesive, a plurality of internal leads formed at regular intervals along the circumference of the chip paddle and conductive wires for electrically connecting the bond pads of the semiconductor chip to the internal leads. A package body comprises the semiconductor chip, the conductive wires, the chip paddle and the internal leads that are preferably encapsulated by an encapsulation material. The chip paddle, the internal leads and the tie bars are externally exposed at their side surfaces and bottom surfaces. The chip paddle is half-etched over the entire upper surface of the chip paddle, which results in a thinner thickness than the internal leads. In one version of the invention, the half-etched chip paddle is about 25-75 % as thick as the internal leads. Accordingly, by half-etching the entire upper surface of the chip paddle, the chip paddle itself is made thinner than the internal leads, leading to the slimming of the semiconductor package.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

FIGURE 1 is a cutaway perspective view of a semiconductor package incorporating the improved leadframe assembly of the present invention.

FIGURE 2 shows a cross sectional elevational view of a semiconductor package wherein the semiconductor package has a chip paddle of reduced thickness according to one embodiment of the present invention; and

FIGURE 3 shows a bottom plan view of the semiconductor package of Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention may be understood more readily by reference to the following detailed description of preferred embodiments of the invention and the figures.

Referring now to Figures 1, 2 and 3, a representative MLF type semiconductor package embodying aspects of the present invention is designated generally 10. Semiconductor package 10 comprises a semiconductor chip 12. Semiconductor chip12 has a plurality of bond pads 14 on an upper surface of semiconductor chip 12 and along a circumference of semiconductor chip 12. A chip paddle 16 is bonded to a bottom surface of semiconductor chip 12 via an adhesive. At a corner of chip paddle 16 is a tie bar 20 (Figures 1 & 2), which extends outwards toward a respective corner of the conductor package 10. Tie bar 20 preferably also has a half-etched portion 21 (Fig. 1).

A plurality of internal leads 22 are located along the circumference of chip paddle 16. The chip paddle 16 and the internal leads 22 are externally exposed at their bottom surfaces (see Figure 2). Additionally, the internal leads 22 are exposed on their side faces (see Figure 1). The externally exposed portions of the chip paddle 16 and the internal leads 22 may be electroplated with a corrosion-minimizing material such as, but not limited to, tin lead, tin, gold, nickel, nickel palladium, tin bismuth, or other similar materials known in the art. Each of internal leads 22 has a half-etched portion 24 at an end facing the chip paddle 16. The upper surface of each of internal leads 22 may also be electroplated with an electrical conductivity enhancing material such as, for example, gold or silver. Conductive wires 26 provide an electrical pathway between the bond pads 14 of the semiconductor chip 12 and the internal leads 22. The semiconductor chip 12,

the conductive wires 26, the chip paddle 16 and the internal leads 22 are encapsulated by an encapsulation material 28 to create a package body 30 whereas the chip paddle 16, the internal leads 22 and the tie bars 20 are externally exposed toward the downward direction of the package body 10. The encapsulation material 28 may be thermoplastics or thermoset resins, with the thermoset resins including silicones, phenolics, and epoxies.

An aspect of the present invention resides in the formation of a half etched surface 32 over the entire upper surface of the chip paddle 16, so as to make the thickness of the chip paddle 16, designated h2 (Figure 2), smaller than the internal lead 22, which is designated h1 (Figure 2). Preferably, the chip paddle 16 is about 25-75 % as thick as the internal leads 22, but this range is presented for example only and should not be construed to limit the present invention.

It is also preferred that the formation of the half-etched surface 32 over the entire upper surface of the chip paddle 16 is conducted while a lower side area of the internal lead is etched, e.g., to form half etched position 24. However, the present invention is not limited to etching the top surface of chip paddle 16 and the half etched position 24 of the internal leads 22 may be formed simultaneously.

By half-etching the entire upper surface of the chip paddle 16, the total height of the semiconductor package body 30 is reduced. When semiconductor chip 12 mounted on the half-etched surface 32 of the chip paddle 16, the semiconductor chip 12 is positioned at lower height than the semiconductor chip 12 would be if it were located on a non-etched chip paddle 16. Thus, the loop height of the conductive wires 26 is also lowered. An additional benefit is that the lower loop height of the conductive wires 26 decreases an occurrence of wire sweeping during encapsulation of the semiconductor package 10. Further, the low height of the semiconductor chip 12 results in decreasing the thickness of the package body 10.

The present invention has been described in an illustrative manner, and it is to be understood that the terminology used is intended to be in the nature of descriptions rather than of limitation. Many modifications and variations of the present invention are possible in light of the above teachings.

As described hereinbefore, the chip paddle 16 is made thinner than the internal leads 22 by half-etching the entire upper surface of the chip paddle 16, so that the total thickness of the semiconductor package 10 can be decreased. In addition, the height of semiconductor chip 12 with respect to the bottom surface of chip paddle 16 is reduced

when the semiconductor chip is mounted on the half-etched chip paddle. Consequently, the loop height of the conductive wires 26 is also lowered, which reduces wire sweeping during the encapsulation of the semiconductor package.

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

Docket No.	Title of Application	First Named Inventor
45475-00013	Improved Thin and Heat Radiant Semiconductor Package and Method for Manufacturing	Jae Hun Ku
45475-00014	Leadframe for Semiconductor Package and Mold for Molding the Same	Young Suk Chung
45475-00017	Method for Making a Semiconductor Package Having Improved Defect Testing and Increased Production Yield	Tae Heon Lee
45475-00018	Near Chip Size Semiconductor Package	Sean Timothy Crowley
45475-00022	End Grid Array Semiconductor Package	Jae Hun Ku
45475-00026	Leadframe and Semiconductor Package with Improved Solder Joint Strength	Tae Heon Lee
45475-00029	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung
45475-00030	Improved Method for Making Semiconductor Packages	Young Suk Chung

It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and the scope of the invention.